ITAP-0012

CONTINUATION OF THE DEVELOPMENT OF FAR INFRARED DETECTION TECHNIQUES

FINAL REPORT

April 1996

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1.0 INTRODUCTION

1.1 Scope

The overall emphasis of the National Aeronautics and Space Administration (NASA) Grant Number NAGW-2864 was to develop technologies required for NASA remote sensing missions operating in the far infrared spectral regions. In this region, the atmosphere of the earth is opaque. Additionally, the high thermal backgrounds from optical systems operating at ambient temperatures severely limit the performance of sensor systems. These constraints can only be fully overcome with cryogenically cooled instrumentation operated in space. The goal of this program was the development of sensors for very low background applications, where sensitivity is the design driver. To this end, this Grant focused on the technology development for the design and demonstration of a cryogenic readout and a 4 x 32 Ge:Ga focal plane array (FPA) module.

1.2 Overview

In the near and mid-infrared (1 - 30 μm), the considerable industrial-based effort over the past two decades has produced arrays as large as 1024 x 1024 elements. In general, these focal planes consist of a two-dimensional array of detector elements that is indium bump bonded to a multiplexer readout. By taking advantage of standard planar microelectronics techniques, this architecture has been used successfully for a large number of arrays. However, the situation at long wavelengths is complicated by a number of technical considerations that make the use of the standard architecture problematical. First, the long wavelengths imply large physical pixel sizes that are not well matched to typical readout die sizes. For example, even a modest 32 x 32 FPA operating at 100 μm would require an array of perhaps 2 cm on a side. Second, the available photoconductor materials (Ge:Ga) have relatively low absorption coefficients, and the absorption thickness must be several mm. For a typical transparent electrode configuration, the charge collection efficiency is poor for a detector this thick. Finally, far-infrared detectors must be cooled to very low temperatures to have adequate dark current performance. To meet the Space Infrared Telescope Facility (SIRTF) requirement, the temperature of the detector elements must be kept below 2 K. This degree of cooling is difficult if the readout electronics, which are themselves a source of heat, are interposed between the detector and the cold sink. For these reasons, Z-plane architectures have been the focus for the far infrared array.

In earlier Multiband Imaging Photometer for SIRTF (MIPS) designs, the detector arrays consisted of single strips of Ge:Ga that were photolithographically delineated into 32 elements. The detectors were interconnected to Amber AE-152 readouts by a variety of novel techniques that provided thermal isolation between the detectors and the readouts. This thermal isolation was necessary because the readouts required an operating temperature above 20 K, well above the acceptable level for the detectors. By stacking these 1 x 32 modules (which were only 0.75 mm thick), arrays as large as 3 x 32 were produced. There were, however, significant difficulties associated with minimizing power dissipation in the readout heaters and preventing excess photon backgrounds from the heated readouts.

1.3 Summary

A 4 x 32 Ge:Ga detector module for use at wavelengths between 50 and 120 μm has been successfully developed by the MIPS Team at the University of Arizona. With 128 elements, this is the largest focal plane array operating in this wavelength range. This array makes use of recently developed low temperature readouts that operate with low noise and good DC stability at temperatures as low as 2 K. We have measured bare multiplexer read noises of 37 e at 4 K for these parts. This module, which has a total power dissipation of 205 μW, forms the basic building block for the 32 x 32 array to be used on SIRTF.

This report describes this new FPA design and its initial test results. In addition, separate test results for the Hughes CRC-696 multiplexer used in this program are presented. Based on these results, performance meeting the SIRTF goal of background-limited imaging can be expected for the 32 x 32 100 μm array.

2.0 INITIAL DEVELOPMENT AND TRADEOFF ANALYSIS

Early FPA designs, developed at the University of Arizona, utilized detector arrays in an 1 x 32 format. These detector arrays, which need to operate at temperatures less than 2 K, were integrated in a thermally isolated assembly using an interconnect that supports and thermally isolates the Amber cascode readout (AE-152) chip which operated at a temperature of 20 K. This interconnect design is discussed below. It was envisioned that these 1 x 32 modules would be stacked to create the 32 x 32 full complement FPA.

2.1 Interconnect Development and Design

The first generation of the 1 x 32 FPA used an interconnect based on a wire leadframe. The leadframe provided a thermally isolated suspension rig which allowed the AE-152 to operate at an elevated temperature independently of the lower detector operating temperature. To ensure optimum detector performance it was important for the detectors to operate at a stable temperature of 2 K for minimum dark current. This technique, while satisfying the core performance requirements, proved labor intensive, extremely sensitive to fabrication tolerances, and difficult to stack. Advanced interconnect technologies were therefore evaluated by the University of Arizona.

Technology development for the second generation 1 x 32 FPA was directed at two interconnection technologies commonly known as flexible circuitry (flex cable) and tape automated bonding (TAB). One goal of this development was to provide a design, fabricate prototype parts, and integrate them into a common 1 x 32 FPA configuration. Another goal was to address the issue of flight qualification of the technology. For this effort, design verification was conducted by way of thermal cycling, mechanical vibration, and electrical testing.

2.2 Construction and Verification Testing

A test plan was established to evaluate interconnects developed by the University of Arizona using both interconnect techniques described in the above paragraph. Details of this can be found in the MIPS Ge:Ga Interconnect Tradeoff Analysis Report, ITAP-0007. A performance evaluation, careful review of design and manufacturing constraints, an assessment of standards, qualification issues, and supplier/material availability reports allowed an interim evaluation of the interconnect technologies described in this document.

From the results of this extensive design, manufacturing, and testing effort, it was concluded that there were no fundamental technological barriers prohibiting the use of either interconnect in a cryogenic environment. It was recommended that further investigation of the interconnect concepts would be required before a down selection could be made. This additional investigation would not only allow a refinement to the concepts as applied to the current generation of readouts, but would also provide a concept evaluation with regard to a future generation low temperature readout.

2.3 Concept Evaluation

An effort was carried out with Hughes Technology Center to review the 1 x 32 module design document in ITAP-0007. HTC was provided with baseline requirements, a drawing package, and performance testing results from the University of Arizona development efforts. HTC was directed to review the module development with the intent of upgrading the design while planning to use the new generation of 2 K readout device. HTC suggested that the flex cable interconnects of the same type used during the tradeoff study could be used in enlarged formats of 4 x 32.

3.0 BREADBOARD DESIGN

3.1 Design Constraints

3.1.1 Cryogenic Operation

One of the keys to the successful development of large format far-infrared arrays has been the construction of readout circuits that operate well at the same temperature as the detectors. Typical silicon MOSFET circuits exhibit a wide range of anomalies when operated below the carrier freezeout temperature of ~20 K. These anomalies are known by many names such as "open substrate syndrome", "kink", "hysteresis", etc. Operationally, the two most serious aspects are a dramatic increase in low frequency noise and a loss of DC stability. Both of these problems would be severe handicaps for an astronomical sensor.

A number of design principles that would minimize the low temperature problems have been defined. The most important of these is the use of a thin, clean, lightly-doped epitaxial layer over a degenerate substrate. By insuring a fully depleted active region, most of the offending behaviors can be avoided. Using the general recipe for the starting material and incorporating a number of proprietary design features, the CRC-696 multiplexer was fabricated at the foundry at Hughes Technology Center, Carlsbad. Six variants of the input unit cell were produced. They are:

a. Source Follower per Detector (SFD)

b. Common Source Cascode (CSC)

c. Capacitive Transimpedance Amplifier (CTIA)

d. Switched Source Follower per Detector (SSFD)

e. Source Follower per Detector, non-segmented (SFD-NS)

f. Auto-zero CTIA (AZ-CTIA)

For the purposes of the focal plane design, the key characteristics of the CRC-696 compared to other readouts are:

a. The readout operates with low noise and excellent DC stability at 2 K.

b. The input capacitance for the bare readout is ~1.5 pF.

c. The 32 input pads are located on one edge of the device at 175 μm centerline spacing.

d. The output and service pads are located on the opposite edge of the device.

e. Nominal power dissipation for the 32-channel device is 64 μW.

The low power dissipation and low temperature operation of the readout is an essential feature of our current design. For the full 32 x 32 focal plane array, the projected power dissipation is 2 mW. To prevent any thermal or photon interference to the detectors, it is necessary to sink this power to the 1.4 K SIRTF heat sink with very little temperature gradient. For example, a rise in detector temperature above 2 K would result in unacceptably high dark currents. Similarly, any non-detector component rising above 4 K would result in an unacceptably high photon background. With this low power dissipation we can provide a large enough thermal path for the readout heat that the temperature remains below 2 K.

3.1.2 Input Capacitance

For all the circuits, minimizing the input capacitance is important for minimizing noise. For the SFD and CSC circuits, reducing the parasitic capacitance is important because the transimpedance of the circuit (the volts out per input charge) is inversely proportional to the total node capacitance. Maximum output swing occurs for the lowest stray capacitance. For the CTIA circuits, the transimpedance is largely set by the feedback capacitor and is hence independent of the input capacitance. The effective gain of the input voltage noise, however, is proportional to the ratio of the input to feedback capacitances. Again, signal to noise ratio is maximized for minimum input capacitance.

Special attention was paid in this design to minimize the input node capacitance. Specifically, the trace length between the detector and the input of the readout was kept at a minimum. Also, a much as possible of the path length is in a low dielectric constant material. The major consequence is in the layout of the detectors. In earlier concepts of the module, each readout serviced a single 1 x 32 detector array. Since the pixel spacing of 750 μm did not match well with the 175 μm spacing of the input pads of the readout, it was necessary to have long fan-in traces on a sapphire substrate to match the two pitches. Traces as long as 15 mm were required in the earlier design. Because sapphire is a high dielectric constant material, the capacitance

penalty was large. A better match would be for each readout to service a 4 x 8 group of detectors. The modest fan out can be accomplished with traces of typically less than 3 mm. The main complication is the need to do multi-layer wire bonding which will be described in a subsequent section. The input capacitance is calculated from the following components in the current design: detector, 0.86 pF; fanout, 0.41 pF; wire bonds, 0.1 pF; readout, 1.5 pF. The total is 2.9 pF.

3.1.3 Thermal Annealing

A well known consequence of operating photoconductors in low backgrounds under ionizing radiation environments is the large change in responsivity of the detectors as a function of ionizing radiation dose. Moreover, the recovery times are long (> 20 minutes) and dependent on background. Since many of the science programs require precise photometric calibration, some form of corrective mediation is necessary. On IRAS the technique of increasing the detector bias above breakdown was used to restore the responsivity to pre-irradiation levels. Flooding the detector with infrared photons is effective and will be used for the ISO Ge:Ga detectors. A third technique which has been found to be the most effective of the three is to thermally anneal the detectors. The recovery rate is exponentially related to the temperature. For Ge:Ga, raising the temperature of the detector above 7 K for only a few seconds is usually enough to restore the responsivity to within a few percent of the pre-irradiation value. The design of the focal plane module supports thermal annealing with the additional constraint that the annealing have a minimal impact on the facility thermal budget.

3.2 Design Description

The Ge:Ga array module consists of four major components as shown in Figure 3-1. The detector assembly consists of a 4 x 32 array of Ge:Ga photoconductors mounted on sapphire fanouts. High purity germanium wedges are mounted in front of the detectors and act as optical concentrators. The electronics assembly consists of a multilayer ceramic board upon which are mounted four readouts, a temperature sensor, and bypass capacitors. The molybdenum frame acts as the overall structural member. Molybdenum was chosen as the material for the frame because of its combination of excellent thermal conductivity and thermal expansion match with sapphire and alumina. The output cable is a standard, single-layer flex cable with copper conductors. All the main components are adhesively bonded with Scotchweld 2216 epoxy.

3.2.1 Detector Assembly

Figure 3-2 provides a cross sectional view of a detector assembly. Each detector assembly is made up of four similar layers. Each layer consists of a metalized and patterned sapphire substrate that acts as a fanout, the 1 x 32 detector array, an undoped germanium optical concentrator, sapphire structural elements, and heater resistors for thermal annealing the detectors.

The detectors are transversely illuminated elements made from Ge:Ga grown at Lawrence Berkeley National Laboratory (LBNL). The top metallization serves as the common bias connection while the individual detector signals are taken from photolithographically delineated lower contacts. The detector contacts are conductive epoxy bonded to individual traces on the sapphire fanout, which carry the signals to bonding pads at the edge of the fanout. The overall dimensions of the Ge:Ga bar are 25.5 mm long, 0.5 mm thick (inter-electrode distance), and 2 mm in the optical absorption direction. There are, in fact, 34 delineated detector positions, but the end elements only serve as optical guard elements.

With a detector active area of 750 μm x 500 μm, but a desired pixel pitch of 750 μm x 750 μm, the fill factor of this array would be unacceptably low. The optical concentrators improve the fill factor significantly by acting as solid photon funnels that direct radiation that would otherwise fall into inactive regions onto the detector. A key to making the optical concentrators efficient is good control of the interface between the concentrator and the detector. The interface can be treated as a simple multilayer dielectric stack of refractive indices 4.0 (Ge concentrator), 1.54 (epoxy filling), and 4.0 (Ge detector). The transmission of this type of stack depends on wavelength, the relative refractive indices, and the thickness of the low-index layer. Good broad band response can be obtained if the two Ge surfaces are flat, smooth, and contacted with less than a 3 μm gap. Alternatively, a controlled gap allows one to "tune" the detector for maximum response at a particular wavelength. The epoxy used for the filling (Epoxy Technology 301) has been measured to have negligible far infrared absorption in the thickness of interest.

Each fanout layer has a pair of thin-film chip resistors mounted near the detectors. These resistors are used to briefly heat the photoconductors briefly to 7 K to remove the effects of ionizing radiation. During the heat cycle, the primary thermal resistance between the detectors and the 1.6 K sink is the epoxy joint between the detector assembly and the molybdenum frame. Finite element thermal transient analysis shows that this design meets the requirement of being able to achieve the anneal temperature for 10 seconds every 30 minutes using a power dissipation of less than 1 mW averaged over 24 hours. Because of the small heat capacities at these very low temperatures, the transient response of the detector assembly is excellent, and the impact on observing efficiency due to thermal anneals should be minimal (See Figure 3-3).

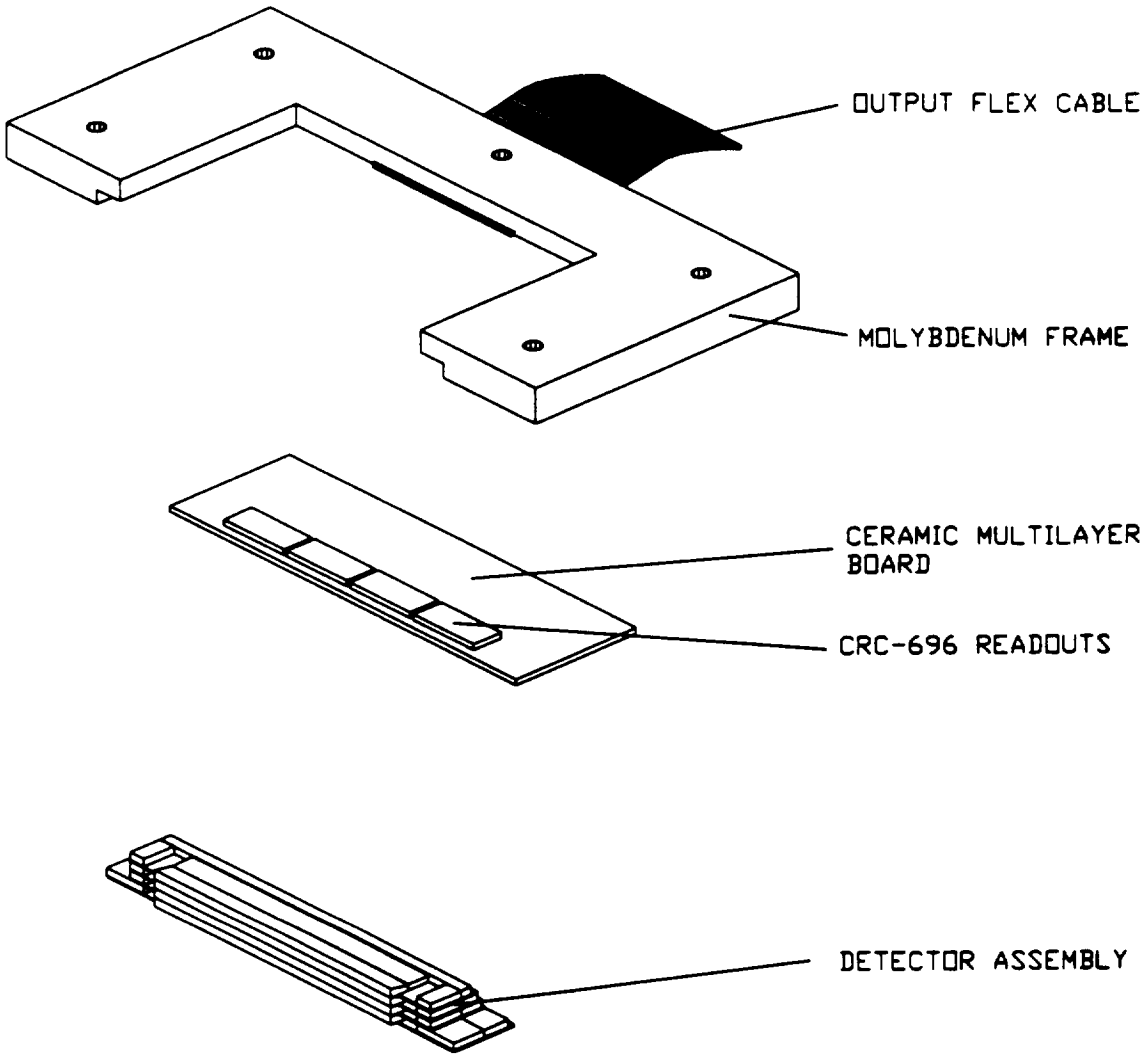

Figure 3-1 Main Components of Ge:Ga Focal Plane Module

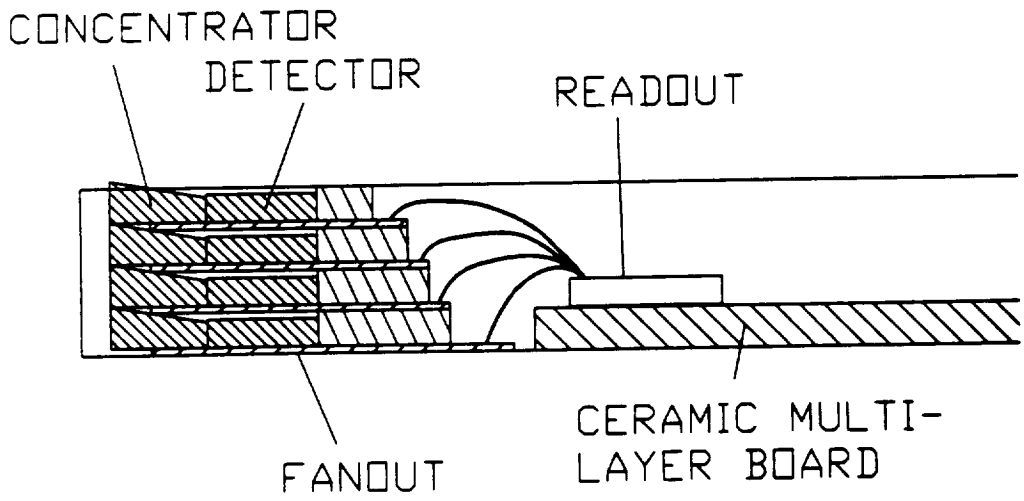

Figure 3-2 Cross Section of Ge:Ga Detector Assembly

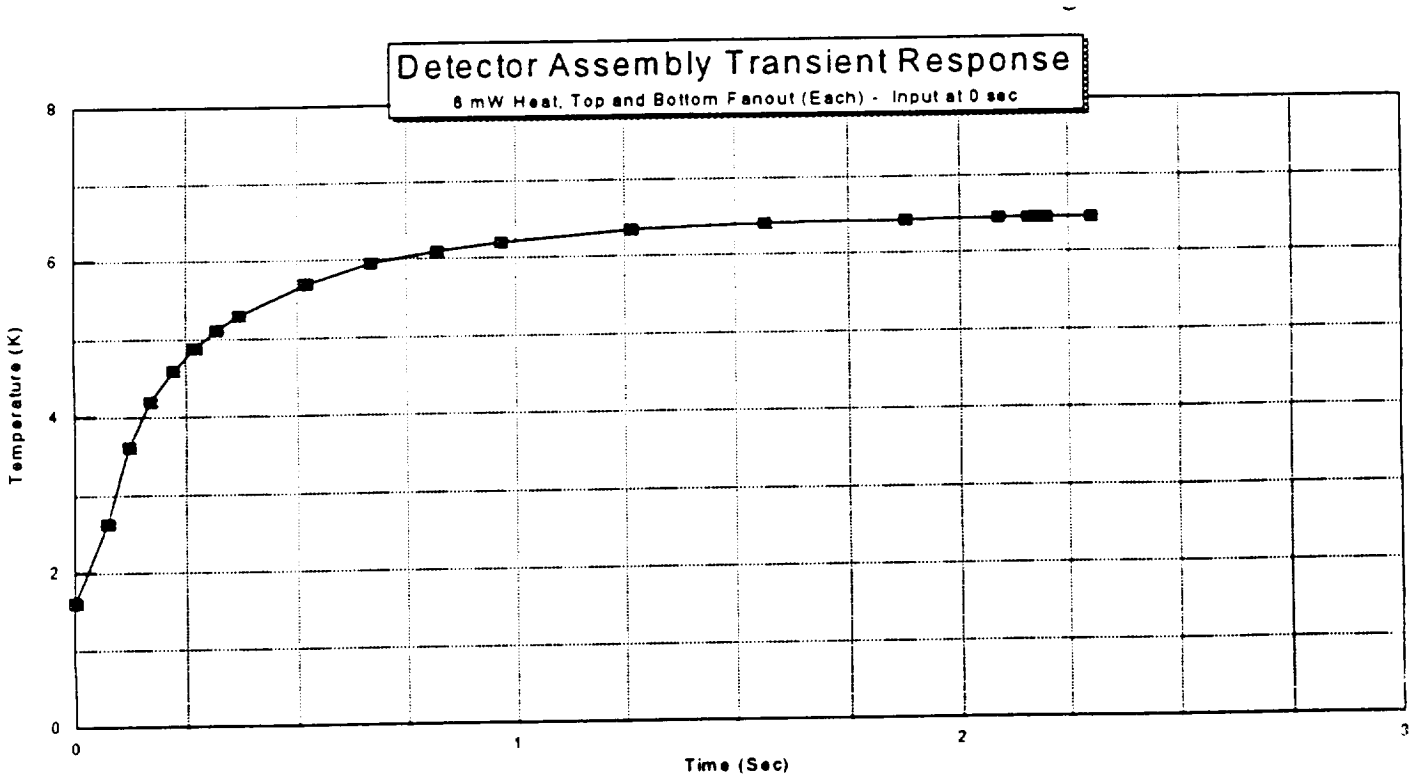

Figure 3-3 Transient Response of Detector Assembly To Thermal Anneal

The depth (along the photon absorption direction) of a given fanout layer is 0.5 mm smaller than that of the layer below it. When the four layers are bonded together, the output pads for all four layers are presented in a stair-step arrangement. Wire bonds directly from the fanout pads to the readout input pads accomplish the electrical interconnect with a minimum of stray capacitance. This mode of multi-level wire bonding requires the use of a deep access bonder, but the techniques are entirely conventional. By careful attention to assembly jigging, the overall height of the four-layer stack is maintained within 25 μm of the nominal 3.05 mm height. This control of height is important for the Z-plane stacking.

3.2.2 Electronics Assembly

The electronics assembly consists of a multilayer ceramic board with four readouts mounted to it. The board has separate conductor layers for the low level analog signals, a ground plane, the digital signals, and the service lines. By separating the digital and analog lines, clock feedthrough to the sensitive lines is minimized. All the supply and address lines for the four readouts are commoned, but each readout has a dedicated output line.

One feature of the ceramic board layout is the avoidance of any layer to layer vias. In previous cryogenic applications, vias have sometimes had reliability problems. In the current design, vias are avoided by running the lines in a serpentine pattern the brings signals to each chip without crossovers. By placing the windows in the dielectric layers at appropriate places, the four readouts can have access to the same commoned traces.

The four CRC-696 readouts are attached to the ceramic board with Scotchweld 2216 epoxy. Also attached to the multilayer board are a temperature sensor and chip bypass capacitors. Electrical interconnects are made with conventional Al-2%Si wire bonds. The Al-2%Si wire is used to minimize the thermal conductance between the readouts and the detector assembly.

3.2.3 Frame

The frame consists of a single milled piece of molybdenum. Molybdenum has a suitable combination of low thermal expansion coefficient along with excellent thermal conductivity. To minimize thermal interface resistance's, the frame is gold plated. The total thickness of the frame is 3.05 mm, the same as the height of four pixel rows. Again, careful attention to the thickness tolerance allows the stacking of multiple modules to form larger arrays.

3.2.4 Output Cable

The output cable is of conventional flex design. The cable is made up of Kapton dielectric with 37 copper conductors. The frame end of the cable has wire bond pads for interconnection to the ceramic board. The other end of the cable terminates in a Nano-series connector.

3.2.5 Assembly

The design allows separate sub-assemblies to be put together and tested independently. In particular, the frame, electronics assembly, and output cable can be integrated into a functional unit. This electronics module can then be cryogenically tested to insure that properly performing readouts have been installed. In particular, low noise at cryogenic temperatures can be verified prior to committing the relatively expensive detector assembly. Similarly, the detector assembly can undergo a room temperature continuity tests to verify the quality of the conductive epoxy bonds.

The choice of a 4 x 32 format for the basic building block has obvious mechanical advantages over the previous 1 x 32 concept. The maintenance of the overall thickness tolerance would be difficult with thirty-two 1 x 32 modules. The error propagation with only eight layers is certainly much less. Moreover, with the 4 x 32 module, the frame is thick enough to maintain a significant amount of mechanical integrity.

4.0 TEST RESULTS

4.1 Cryogenic Readouts

SFD and CTIA circuits from both lots have been tested. For these tests, the devices are mounted in 68-pin leadless chip carriers with the inputs open. For the SFD circuit, additional capacitance on the input node associated with the detector and interconnect will reduce the output voltage to input charge transfer ratio. For the CTIA, the effective gain of the input voltage noise will increase with increasing capacitance. Hence, the quoted read noises must be scaled to get the noises in actual operation with a detector. The read noise is computed using the linear regression method. Because the multiplexers allow non-destructive readout, multiple samples for each channel were taken and a least squares linear fit through the data points to derive the slope is done. Typically for each channel 64 samples at 8 samples per second for each integration are taken. The read noise is defined as the standard deviation of an ensemble of slope measurements multiplied by the integration time. The 8-second integration time is expected to be typical for the SIRTF far infrared arrays since significantly longer times between resets are precluded by cosmic ray hits.

Devices were tested at both 77 K and 4.2 K. Devices from both lots showed excellent behavior at deep cryogenic temperatures. To determine the optimum power dissipation, noise as a function of device current was measured. For the CRC-696, the device current was easily varied by changing the voltage on a current mirror. For both lots, the optimum current is just above 0.3 μA per channel. Below this value, increases in the low-frequency noise are observed while much higher currents yield no benefits in noise performance.

Table 4-1 shows "typical" results from our test program. We have found that the read noise for the CTIA at 4.2 K has somewhat higher dispersion that would be expected from the SFD data. Noise on a given part could be a factor of 1.2 larger or smaller than the typical value. No significant differences have been seen between the two lots other than slightly higher noise for the second run, and a requirement for a higher substrate potential for the second run. At this point we do not have sufficient data to identify significant differences between the 2 μm and 3 μm epi thicknesses.

The devices show excellent uniformity in offsets. For a given 32-channel multiplexer, the peak-to-peak variation in offsets is usually less than 2 mV, with some devices showing less than 1 mV variation. This level of uniformity means that auto-zero circuits are unnecessary for CTIA's.

Table 4-1 Bare Multiplexer Test Results

Device	Lot	Read Noise 77 K	Read Noise 4.2 K
SFD	3	20 e	37 e
SFD	5	25 e	45 e
CTIA	3	15 e	40 e
CTIA	5	19 e	50 e

4.2 Array Tests

4.2.1 1 x 32 Results

To get an early measurement of the behavior of the CRC-696 readout with Ge:Ga detectors, we constructed a 1 x 32 array based on an older, heated readout concept. The design is based on a flex cable interconnect. The linear detector array is mounted on a thin sapphire fanout. The connection between fanout and the readout is made with a Constantan conductor flex cable. The readout is mounted directly to the flex cable which provides both thermal isolation and mechanical support. Because heated operation was unnecessary for the CRC-696, the region of the readout was thermally strapped to the 2 K heat sink.

Tests were conducted using both flood illumination and spot illumination. Under flood illumination the array uniformity is better than 20% over the 25 mm length of the Ge:Ga bar. This level of response non-uniformity is easily corrected by taking flat fields. The array was also illuminated with a "spot" source. The spot illumination was created by placing a small aperture directly in front of the array and illuminating it with the flood source. Figure 4-1 shows the response of the array under these conditions. The level of crosstalk is high but not unexpected given the significant amount of capacitive coupling in the flex cable. The design is optimized in the following 4 x 32 array. Table 4-2 summarizes the results for the interim 1 x 32 array. Note that the performance values are compromised by the high input node capacitance for this non-optimized configuration. Despite these shortcomings, the results showed that with a lower capacitance front end, significant improvements in array performance could be expected with an architecture optimized for the CRC-696.

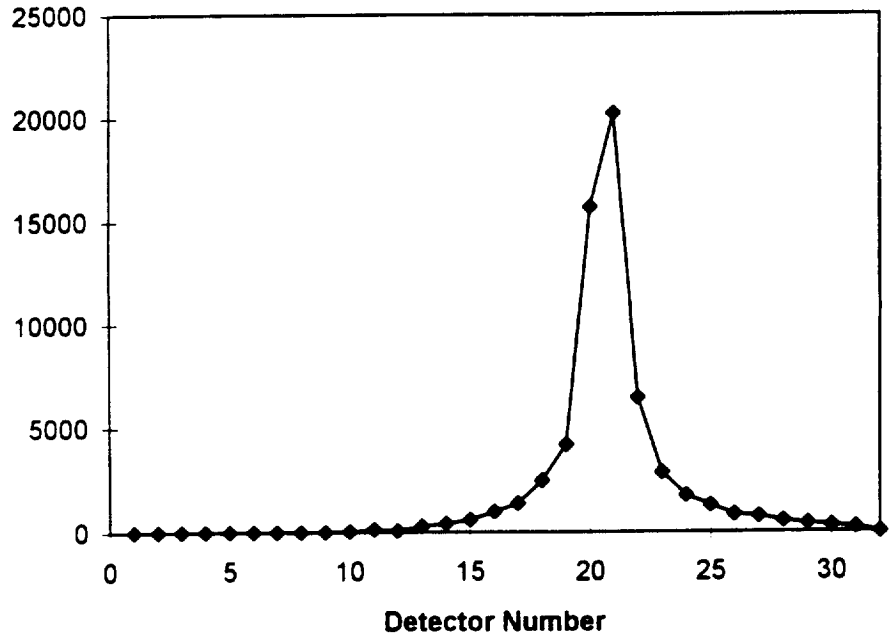

Figure 4-1 1 x 32 Spot Illumination

Table 4-2 Test Results for 1 x 32 Array

Power Dissipation	64 μW
Dark Current	< 350 e/s
Read Noise	120 e
Input Node Capacitance	6.4 pF
Detector Non-Uniformity	20%

4.2.2 4 x 32 Array Module

The initial tests were conducted in a test dewar normally used for dark current measurements. To provide a simulation of point sources, an aperture mask was placed approximately 0.5 mm in front of the array with four 0.7 mm diameter holes. An Infrared Laboratories thermal stimulator provided the infrared flood illumination source.

One of the concerns with the use of exposed multiplexers with sensitive infrared sensors is the possible presence of "amplifier glow". This phenomenon is attributed to an LED-like emission in the transistors of the readout, particularly elements that draw substantial current like output drivers . On large format indium bump bonded arrays, this problem usually manifests itself as an excess dark current that is correlated with particular operational modes. The dark current measured for the array is less than 400 electrons/s despite the fact that no heroic efforts to shield the readouts from the detectors have been made in this design. The implication is that at the very low voltages applied to the transistors (typical source-drain voltages are 0.7 V), the amount of amplifier glow is negligible.

Power dissipation for the 4 x 32 module is 0.4 μA x 2 V x 128 channels = 205 μW. For the full 32 x 32 array, the power dissipation would be 1.6 mW, well within the goal of less than 5 mW. We have found that increased power dissipation does not improve the low frequency noise performance of the readout, while cutting the power dissipation in half results in an increase in read noise.

In the MIPS instrument, the focal plane array will be buried deep within the cryostat. An important systems consideration is the ability of the readout to drive long cables without the aid of a separate line driver. We have tested the capability of the CRC-696 to drive long miniature coaxial lines. No waveform distortion is encountered when driving 3 meters of ultra-miniature stainless steel coaxial line. This cable has an outer jacket diameter of 1.0 mm and a capacitance of 174 pF/m.

Figure 4-2 shows the results of the first imaging tests done with the 4 x 32 array. Photocurrents in the brightest spots are approximately 20,000 e/s while in the darkest regions, the photocurrents are below 500 e/s.

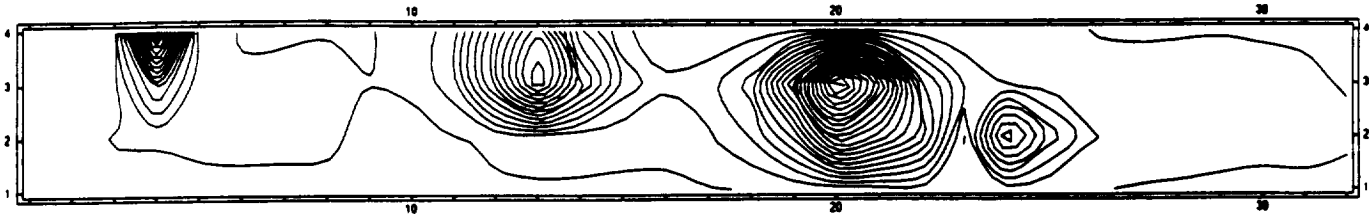

Figure 4-2 Spot Illumination Image With 4 x 32 Ge:Ga Array

5.0 ABBREVIATIONS AND ACRONYMS

Al	Aluminum
AZ-CTIA	Auto-zero Capacitive Transimpedence Amplifier
CSC	Common Source Cascode
CTIA	Capacitive Transimpedence Amplifier
DC	Direct Current
e/s	electron/second
FPA	Focal Plane Array
Ge:Ga	Gallium Doped Germanium
IRAS	Infrared Astronomical Satellite
ISO	Infrared Space Observatory
K	Kelvin
LBNL	Lawrence Berkeley National Laboratory
M	Meter
MIPS	Multiband Imaging Photometer for SIRTF
mm	millimeter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
mV	millivolt
mW	milliwatt
NASA	National Aeronautics and Space Administration
pF	pico-Farad

S	Second
SFD	Source Follower per Detector
SFD-NS	Source Follower per Detector, non-segmented
Si	Silicon
SIRTF	Space Infrared Telescope Facility
SSFD	Switched Source Follower per Detector
V	Volt
μA	microamp
μm	micron
μW	microwatt